FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE (REV. 7-80) PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.: 57941.000013	SERIAL NO.: 10/673.677
	INVENTOR'S NAME: Jared LeVan ZERBE et al.	EXAMINER: Unassigned
LIST OF MATERIALS CITED BY APPLICANT (Use several sheets if necessary) Page 1 of 1	FILING DATE: September 30, 2003	GROUP: Unassigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS AND SUBCLASS	TRANSLATION PROVIDED	
						Yes	No

		OTHER MATERIALS (Including Author, Title, Date, Pertinent Pages, Etc.)
SL	1.	M. RAU et al., "Clock/Data Recovery PLL Using Half-Frequency Clock," IEEE Journal Of Solid-State Circuits, Vol. 32, No. 7, July 1997, pp. 1156-1159
SL	2.	CHIH-KONG et al., "A 0.8-μm CMOS 2.5 Gb/s Oversampling Receiver and Transmitter for Serial Link," IEEE Journal Of Solid-State Circuits, Vol. 31, No. 12 December 1996, pp. 2015-2023
SL	3.	RAMIN FARJAD-RAD et al., "A 0.3-μm CMOS 8-Gb/s 4-PAM Serial Link Transceiver," IEEE Journal Of Solid-State Circuits, Vol. 35, No. 5, May 2000, pp. 757-764
SL	4.	KUN-YUNG KEN CHANG et al., "A 0.4-4Gb/s CMOS Quad Transceiver Cell using On-chip Regulated Dual-Loop PLLs," 4 pages 2002.

EXAMINER	/Siu Lee/	DATE CONSIDERED	01/08/2007

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